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Patents Publication number High bandwidth memory interface: US8661285: Jun 29, 2011: Feb 25, 2014: Uniquify, Incorporated: Dynamically calibrated DDR memory

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Hyun-Woo Lee; Recently, the memory interface has been improved up to 20Gb/s/link [1]. signaling for high-speed parallel electrical links.

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Developing high-speed memory interfaces: the

DEVELOPING HIGH-SPEED MEMORY INTERFACES: design high-speed memory interface solutions. high bandwidth memory devices with a high

Patent us20150078057 - high bandwidth memory

Several generations of high bandwidth DRAM-type memory devices an improved high bandwidth chip-to-chip interface for Service - About Google Patents

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interface and packaging standards for many generations from the very beginning of semiconductor memory including DRAM, HIGH BANDWIDTH MEMORY (HBM) DRAM: JESD235

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High-Bandwidth Memory Interface. Chulwoo Kim Hyun-Woo Lee, Chulwoo Kim. IEEE Trans. VLSI Syst., 22(4)

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IEEE Standard for High-Bandwidth Memory Interface Based on Scalable Coherent RamLink is an applicable interface for other RAM-like devices as

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